TOHOKU UNIVERSITY
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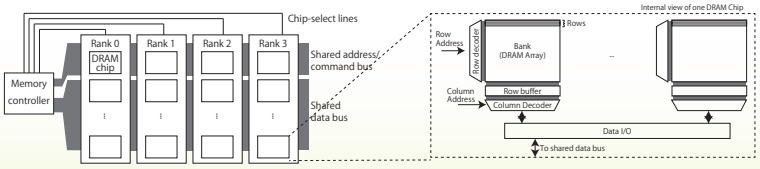
An Energy-Efficient Dynamic Memory Address Mapping Mechanism

Introduction

DRAM-based Main Memory

Reducing the energy consumption of DRAM-based main memories becomes one of the major issues on reducing total energy consumption of the whole system.



The DRAM access protocol

1. Precharge: preparing a bank to read data
2. Row activation: storing data in the entire row to the row buffer of the bank
3. Column read/write: selecting column in the row and read/write data
   * Steps 1 and 2 can be omitted in the case of reusing the row buffer contents

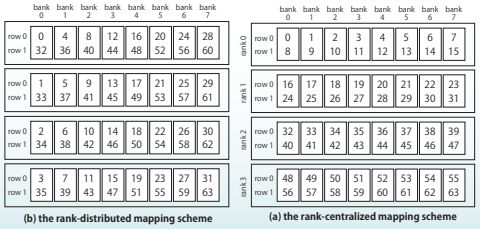
The DRAM low-power mode

Inactivates decoders and data I/Os per rank if there is no access for a certain time

The low-power mode is requisite for reducing the energy consumption of DRAM-based memory systems

Address Mapping Schemes

The schemes determine the data location on DRAM by using physical addresses of data.



(b) the rank-distributed mapping scheme (a) the rank-centralized mapping scheme

The scheme that can achieve less energy consumption than the other scheme is different depending on the memory access characteristics of executed applications

Example: Accessing the data whose address ranges from 0 to 3

	The rank-centralized scheme	The rank-distributed scheme
Power	Low power consumption (accessing only Rank 0)	High power consumption (accessing Ranks 0 to 3)
Performance	Low performance (hazard in intra-rank hardware)	High performance (rank access can be interleaved)

Impacts of Energy Consumption of the Address-mapping Schemes

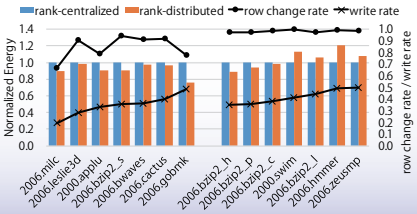
The energy efficiency of the memory system is depending on how much the rank-distributed scheme can be beneficial by reusing the contents of the row buffers that consume a large energy.

Key Metrics

Row change rate
= (accesses to a different row from the previous access) / (all accesses)
High row change rate reduces the number of reuses on row buffers

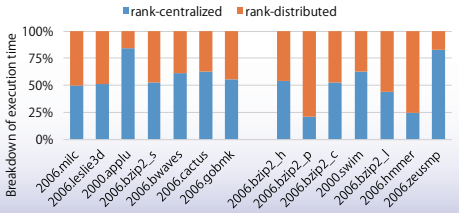
Write rate = (Write accesses) / (all accesses)
High write rate enlarges the performance impact of the write-to-read latency, which costs latency for two consecutive write/read to the same row.

Energy Consumption



The rank-centralized scheme can achieve less energy than the other when (write rate > 40%) and (row change rate > 95%)

Breakdown of Time Suitable for Each Scheme



Each application includes phases suitable for both of the schemes

*These results are obtained by simulating 8GB 4-rank DDR3-SDRAM

Dynamic Memory Address Mapping Mechanism

Basic Idea

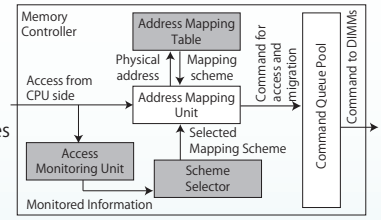
Dynamically switching the address-mapping scheme between the two schemes so that the selected scheme achieves less energy consumption than the other scheme.

Memory Controller Organization

Address-Mapping Table: records which scheme stores the data, indexed by physical address

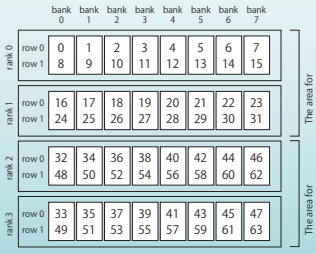
Access Monitoring Unit: monitors memory accesses and calculates the row change rate and the write rate

Scheme Selector: determines which scheme can reduce energy based on the row change rate and the write rate



Memory Space Partitioning

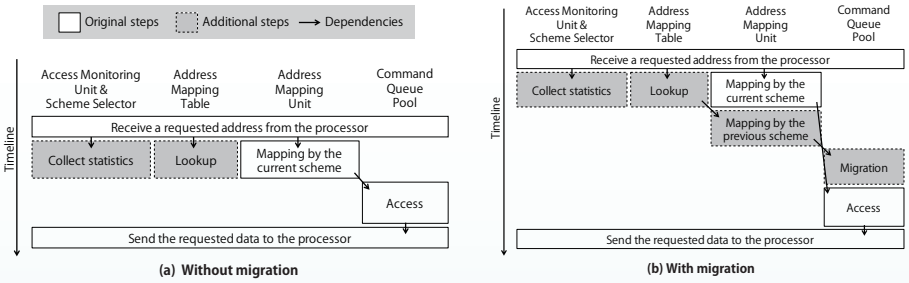
This partitioning prevents the multiple data from being allocated to the same place



If the data whose addresses range from 0 to 3 need to be migrated to the area of rank-distributed scheme, the data can be migrated to 32, 33, 34, and 35, with swapping the data contents.

Memory Access Procedure

The controller also processes the data migrations only when the data is accessed and if the migration of the data should be done.

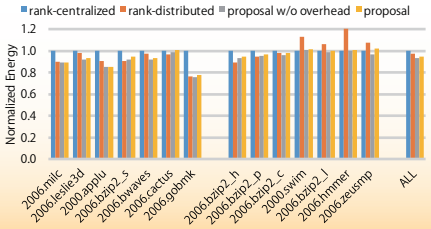


(a) Without migration (b) With migration

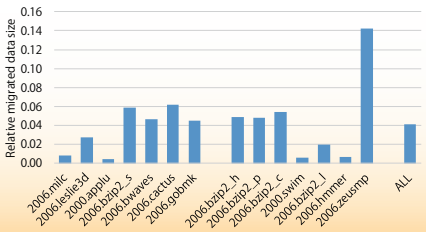
Evaluations

- An appropriate mapping scheme is determined every 100,000 memory cycles.
- The scheme is changed every 8KB block, which is unit of data migration. The migration cost is included as the overhead
- The address-mapping table has 1MB entries, each of which needs 1bit, included as the overhead

Energy Consumption



Migrated Data Size



22% and 16% reduction from the rank-cent. and rank-dist. schemes, respectively
The overhead of migrations does not negate the beneficial effect of the proposed mechanism.

Conclusions

- DRAM-based main memories consume a large energy cosumption, and it is required to reduce their energy consumptions.
- To reduce the energy consumption of main memories, the dynamic memory address mapping mechanism is proposed.
- Future Work: The thresholds to judge the suitable schemes should be quantitatively estimated by DRAM specifications.

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