



Optimizing Memory Layout of Hyperplane Ordering for Vector Supercomputer SX-Aurora TSUBASA

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Background and Motivation

- · Various phenomena in the real world can be reproduced more realistically by large-scale simulations using supercomputer systems.
- There are still many issues to be addressed in the real world, and the impact of problems with social infrastructures (ex. gas and steam turbines) on our society is immeasurable.

Numerical Turbine Code

Necessary to conduct a numerical simulation of a turbine using a supercomputer to simulate various phenomena occurring in the turbine in order to predict such failures in advance.

3D Hyperplane

Vector Gather on

Vector Scatter op



Indirect Access

162

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Tohoku University



The time integration routine uses the LU-SGS scheme. A hyperplane ordering method is adopted for vectorization.

Proposal - Optimizing Memory-access Pattern -

Specification of SX-Aurora TSUBASA

SX-Aurora TSUBASA (Vector Engine: Type 10B)	
Form Factor	
Vector Length	256 elements (16k bits)
Vector Cores	8
Frequency	1.4GHz
Flops/core	268.8GF (DP)
Flops/processor	2150.4GF (DP)
Cache Capacity	16MB (shared)
Mem. Bandwidth	1.2TB/s
Mem. Capacity	48GB

Full-annulus Simulation by Numerical Turbine

> The maximum vector length of SX-Aurora TSUBASA is 256. Applications should have long loop lengths to exploit the high performance.

- 3D hyperplane provides long vector lengths.
- The method is accompanied by a high memory load.

Our proposed 3D hyperplane can reduce indirect accesses by changing the data layout.



228

20

Long

Evaluation Results



Full Application (Numerical Turbine Code)



The proposed method impoves the performance by up to 2.77x, and 1.27x on average, compared with the original (3D hyperplane).

Conclusions and Future work

• The 3D hyperplane ordering method is suitable for SX-Aurora TSUBASA because the method can provide long vector lengths.

- Our proposed 3D hyperplane ordering method further improves the performance by reducing indirect memory accesses.
- Future work: examine the effect of the method on other applications and widly used SIMD architectures.

SC19 Denver, Colorado

(URL) https://www.cal.is.tohoku.ac.jp (E-mail) osamu.watanabe.t5@dc.tohoku.ac.jp